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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/091,925 | 03/06/2002 | Kazuto Nishimura | FUJY 19.478 | 7074 |

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| EXAMINER | |
|---|---|
| WONG, WARNER | |
| ART UNIT | PAPER NUMBER |
| 2668 | |

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/091,925 | NISHIMURA ET AL. | |
| | Examiner | Art Unit | |
| | Warner Wong | 2668 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-14 and 16-20* is/are rejected.

7)☐ Claim(s) *5 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. The following claims are objected to because of the following informalities:

**Claim 1, line 2**: The limitation "nodes" appear to be referring to the same limitation "insertion nodes" described in lines 4-5. It should be reworded to "insertion nodes".

Claim 1, lines 4-5: The limitation "storage areas according to insertion nodes" appears to be referring to the same limitation "every-insertion-node oriented storage area" as describe in subsequent claims and specification. Hence it should be reworded to ""every-insertion-node oriented storage area" to avoid confusion.

**Claim 4, line 3**: The phrase "each others" should be grammatically corrected as "each other".

**Claim 9, lines 3-4**: The limitation "the insertion node number" lacks antecedent basis. It should be changed to "an insertion node number".

**Claim 10, lines 6**: The limitation "the insertion node number" lacks antecedent basis. It should be changed to "an insertion node number".

Appropriate correction is required.

### *Specification*

2. 35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms which are not clear, concise and exact. The specification should be revised carefully in order to

comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are:

The limitations "a storage unit" and "storage areas" appear to be used interchangeably with the terminologies "every-insertion node oriented buffer unit" and individual buffer memory" respectively throughout the specification and claims in view of the specification descriptions and drawings. The specification and the claims should be rewritten to use the same limitation terminologies to avoid confusion and ambiguity.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6-7, 9-14, 16-17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mekkittikul (2005/0249128) in view of Kilkki (6,219,351)

**Regarding claim 1**, Mekkittikul describes:

a node (fig. 3, MPS switch #304) in a ring network system in which a plurality of nodes are connected in loop through a ring transmission path (fig. 3, and where the packets are inserted into the ring transmission path).

a read control unit reading the packets in a fair way on the basis of predetermined weights respectively from said storage areas according to said insertion nodes (paragraphs 42-44, where the buffer controllers 314-316 is the read control unit,

and the fair bandwidth allocation scheme evaluates on the basis of predetermined/allocated weights w[i]).

Mekkittikul lacks what Kilkki describes:

a storage unit having storage areas [according to insertion nodes] at which arrived packets are (inserted into) output (path) (fig. 6 and col. 5, lines 21-26, where storage areas are the output buffers OBF[1..n] and the aggregate of the OBF's is the storage unit), and accumulating the packets in said storage areas according to said insertion nodes (col. 2, lines 53-56, where individual FIFOs are deployed to accumulate packets destined to a corresponding output [destination], i.e. another insertion node).

It would have been obvious to one with ordinary skills in the art at the time of invention by applicant to deploy the buffering used by Kilkki into the node of Mekkittikul. The motivation being that "the switch must have buffering capacity to avoid the necessity of discarding cells in such a situation", col. 2, lines 8-10.

4. **Regarding claim 11**, Kilkki describes a packet control method, comprising:

a ring network system in which a plurality of nodes are connected in loop through a ring transmission path (fig. 3).

reading the packets in a fair way on the basis of predetermined weights respectively according to said insertion nodes (paragraphs 42-44, where the buffer controllers 314-316 uses a fair bandwidth allocation scheme to evaluate transmission packet flows on the basis of predetermined/allocated weights w[i]).

Mekkittikul lacks what Kilkki describes:

a provision of storage areas (output buffers) according to insertion nodes at which arrived packets are (inserted into) output (path) (fig. 6 and col. 5, lines 21-26, where storage areas are the output buffers OBF[1..n]), and accumulating the packets in said storage areas according to said insertion nodes (col. 2, lines 53-56, where individual FIFOs are deployed to accumulate packets destined to a corresponding output [destination], i.e. another insertion node);

It would have been obvious to one with ordinary skills in the art at the time of invention by applicant to deploy the buffering used by Kilkki into the node of Mekkittikul. The motivation being that "the switch must have buffering capacity to avoid the necessity of discarding cells in such a situation", col. 2, lines 8-10.

**Regarding claims 2 and 12**, Mekkittikul and Kilkki combined describe all limitations set forth in claims 1 and 11 respectively. Kilkki further describes:

an identifying unit identifying said insertion node at which the packets are inserted into said ring transmission path on the basis of specifying information contained in the packet (INW switch of fig. 6 and col. 5, lines 22-23, where the INW switches/identifies packets destined for a particular output/insertion node on the basis of the routing tag).

an accumulation control unit (fig. 6, BMs) accumulating the packets in the corresponding every-insertion-node oriented storage area (fig. 6, OBF[1..n]) on the basis of a result of identifying said insertion node (fig. 6 and col. 5, lines 22-23, after INW switches/identifies the destination/output port of the packet).

**Regarding claims 3 and 13**, Mekkittikul and Kilkki combined describe all limitations set forth in claims 1 and 11 respecitvely. Mekkittikul and Kilkki combined further describe a storage module stored with mappings (Kilkki, fig. 6, table) between uniform weight values (Mekkittikul, paragraph 48, example of queues of uniform weight) as the predetermined weights and said insertion nodes (Kilkki, fig. 6, VPI/VCI of packet) (Kilkki, fig. 6 and col. 5, lines 12-15, where the table column of delay "DP" value, which maps to VPI/VCI of packets, may be replaced with the uniform weight values of Mekkittikul, paragraph 48).

**Regarding claims 4 and 14**, Mekkittikul and Kilkki combined describe all limitations set forth in claims 1 and 11 respectively. Mekkittikul and Kilkki combined further describe a storage module stored with mappings (Kilkki, fig. 6, table) between different weight values (Mekkittikul, paragraph 48, "The weight of each queue allows the implementation of different levels of bandwidth per queue") as the predetermined weights and said insertion nodes (Kilkki, fig. 6, VPI/VCI of packet) (Kilkki, fig. 6 and col. 5, lines 12-15, where the table column of delay "DP" value, which maps to VPI/VCI of packets, may be replaced with the different weight values of Mekkittikul, paragraph 48).

**Regarding claims 6 and 16**, Mekkittikul and Kilkki combined describe all limitations set forth in claims 4 and 14 respectively. Mekkittikul and Kilkki further describe that the weight values different from each other as the predetermined weights are proportional to a total sum of reserved bandwidths of the connection for inserting the packets (Mekkittikul, paragraph 47, "The queues of each MPS track the data traffic

belonging to each individual flow" and paragraph 48, "The queues are emptied at a rate affected by their respective weight, W[i]).

**Regarding claims 7 and 17**, Mekkittikul and Kilkki combined describe all limitations set forth in claims 4 and 14 respectively. Kilkki and Mekkittikul further describe:

every-insertion-node oriented storage area (Mekkittikul, fig. 3, #322-324) of said storage unit (Mekkittikul, fig. 3, #304) is physically segmented into a plurality of areas (Mekkittikul, paragraph 42, "Each of these computers 308-310 has a corresponding [separate] buffer 311-313), and said accumulation control unit (Kilkki, fig. 6, BM) permits only the packet from said corresponding insertion node to be written to each of the segmented areas of the every-insertion-node oriented storage area (Mekkittikul, fig. 3, #322-#324 and paragraph 42, where only the personal computer/user may insert packets to the its corresponding buffer).

**Regarding claims 9 and 19**, Mekkittikul and Kilkki combined describe all limitations set forth in claims 2 and 12 respectively.

Kilkki further describes: the identifying unit (switch) identifies said insertion node at which the packet is inserted into said ring transmission path on the basis of the insertion node number (routing tag) as the specifying information contained in the packet (col. 5, lines 22-23, where the switch identifies the destination by the routing tag of the cell.)

**Regarding claims 10 and 20**, Mekkittikul and Kilkki combined describe all limitations set forth in claims 2 and 12 respectively.

Kilkki further describes: a storage module (fig. 6, table) stored with mapping between traffic identifiers of the packets (fig. 6, VPI/VCI) and the insertion node numbers (fig. 6, routing tags) and wherein said identifying unit (switch) identifying said insertion node at which the packet is inserted into said ring transmission path on the basis of the insertion node number corresponding to the traffic identifier, as the specifying information contained in the packet (col. 5, lines 22-23, where the switch identifies the destination by the routing tag of the cell), which is obtained by referring to said storage module (col. 5, lines 18-21).

5. **Claims 8 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mekkittikul in view of Kilkki as applied to claims 2 and 12 above, and further in view of Mansour (2003/0067931).

Mekkittikul and Kilkki combined describe:

every-insertion-node oriented storage area (Mekkittikul, fig. 3, #322-324) of said storage unit (Mekkittikul, fig. 3, #304) is physically segmented into a plurality of areas (Mekkittikul, paragraph 42, "Each of these computers 308-310 has a corresponding [separate] buffer 311-313), and said accumulation control unit (Kilkki, fig. 6, BM) permits only the packet from said corresponding insertion node to be written to each of the segmented areas of the every-insertion-node oriented storage area (Mekkittikul, fig. 3, #322-#324 and paragraph 42, where only the personal computer/user may insert packets to the its corresponding buffer).

Mekkittikul and Kilkki lack what Mansour explicitly describes:

the output buffers (storage areas) are provided by dynamically logically segmenting a shared storage areas (fig. 1, # memory and paragraph 4, "Once inside the memory, packets are organized into separate output queues, one queue for each output line").

It would have been obvious to one with ordinary skill in the art at the time of rejection by applicant to use a shared memory and logically segment it for storage areas instead of having physically separated storage areas. The motivation being that in using one physical shared memory the design may be more economical in design than in using a multiplicity of physical memory.

### *Allowable Subject Matter*

6. Claims 5 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Carrafiello (2002/0159460), Dally (6,654,381), Lyles (5,519,698), Nishimura (6,659,432) and Stiliadis (6,134,217).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Warner Wong whose telephone number is 571-272-8197. The examiner can normally be reached on 5:30AM - 2:00PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Warner Wong
Examiner
Art Unit 2668

WW

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER